IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application No. 10/526,421

Confirmation No. 3287

Applicant: Leijten, Jeroen Anton Johan

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Examiner: Faherty, Corey S.

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop Appeal Brief – Patents
Commissioner for Patents
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Dear Sir:

Appellants request review of the final rejection, dated March 30, 2009, in the above-identified application. No amendments are being filed with this request. This request is being filed with a notice of appeal. An appeal brief has not yet been filed. This Pre-Appeal Brief Request For Review is submitted for the reasons stated on the attached sheets.

REMARKS

Appellant traverses the continued rejection of Claims 1-11, 13 and 15-17 in the Final Office Action dated July 1, 2009. Appellant specifically traverses the rejection of independent claim 1 as being obvious over Downing, U.S. Patent 3,781, 810 (Downing). Appellant believes that there has been a clear error with regard to the application of Downing to independent claim 1, and as a consequence the cited prior art does not disclose or suggest each of the recited elements of presently appealed claim 1.

As clarified in Appellant's amendment in reply to the **Office Action dated July 24, 2007**, the state information saved during the handling of an interrupt condition includes state information from the processor pipeline. However, Downing does not disclose or suggest this feature, thus a *prima-facie* case of obviousness has not been established.

This clear error necessarily impacts the rejections of each of the presently pending dependent claims.

Appellant's Claimed Invention

Appellant's claim 1 recites a data processor including one or more functional units, one or more register files, a data memory, and a snapshot buffer. During handling of an interrupt condition, the snapshot buffer accommodates saving state information of various processor state elements, including state information from the internal processor pipeline formed by the functional units. The claimed data processor includes "controller means" (See controller 26) that, upon entry of an interrupt processing state, save state information of processor state elements (registers) currently with in the snapshot buffer in the data memory facility having the multi-bit access port facility.

Thus, regarding the invention recited in present claim 1, the snapshot buffer differs from the claimed register files and is provided *in addition* to the set of one or more register files. As a consequence, during handling of an interrupt the snapshot buffer receives/saves state information of various processor state elements (registers). The state information includes state information from the internal processor pipeline. During handling of an interrupt condition, information from processor state elements is transferred to the snapshot buffer elements. Furthermore, upon issuance of a subsequent interrupt during processing of a current interrupt, the contents of the

snapshot buffer elements are transferred to the "data memory facility having the multiport facility" (to make room in the snapshot buffer for the state information from the internal processor pipeline)

Downing's Disclosure

Downing discloses a program controlled computer which comprises independent control circuitry for exchanging data between registers R1, ..., Rn of the computer and the computer memory independently of the execution of program. This arrangement saves computer time as it facilitates the storing and retrieving of data which must be saved during nesting and unnesting of program transfers. For each register R1,...Rn that contains data which is to be saved upon the occurrence of a program interrupt, there is provided an auxiliary register AR1,...ARn and program controlled gates for exchanging data between the computer register and its corresponding auxiliary register.

Non-Obvious Differences Between Downing and Appellant's Claimed Invention

In accordance with Appellant's claimed invention the saved state information of various processor state elements includes state information from the internal processor pipeline.

Section 7 of the Office Action states that Downing does not explicitly disclose that the system is pipelined, but that the use and benefits of pipelining are notoriously well known in the art and that the use of the techniques described by Downing in a pipelined processor would therefore have been obvious to a person having skill in the art.

The use and benefits of pipelining are indeed known. In particular, it can be seen in FIG. 2B that the processor 13 known from Downing comprises a pipeline with various internal state elements, including;

SAVR (element 32)
RESR (element 33)
ADDRESS REGISTER (element 16)
POINTER STORE (element 29)
BASE ADDRESS STORE (element 30)
REGISTER ADDRESS STORE (element 44)

Despite the fact that Downing's processor has these state elements, only the data registers R1, ..., Rn comprise a respective auxiliary register that serves to temporarily save the data in the

corresponding data register. No such auxiliary storage is shown for the internal state elements of the processor 13. Hence, while Downing explicitly shows an arrangement comprising a processor with data storage elements as well as internal state elements and explicitly shows auxiliary registers for saving data from the data registers R1, ...,Rn, **Downing does not disclose or suggest that state information from the internal pipeline is saved**.

For example, in the arrangement of Downing as shown in Figure 2B, the elements "base address store 30" and "pointer store 29" form a pipeline with the address register 27.

Before a next subroutine can be carried out this pipeline has to be flushed, otherwise, data of the previous subroutine present in the elements 29, 30 would enter the element 27 when immediately executing the subsequent subroutine.

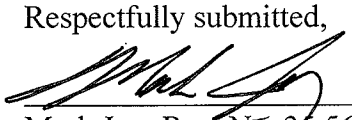
In the present invention as claimed in present claim 1, also the state information of the internal processor pipeline is saved in snapshot buffer elements, thus enabling a context switch in a single clock cycle.

This measure is apparently not obvious in view of the fact that Downing is aware that the processor has an internal state, and that Downing describes a method to save state information during interrupts. Yet Downing fails to recognize that this method could be used to save the internal state of the processor.

Conclusion

Appellant respectfully submits that the patent application is in condition for allowance. If, in the opinion of the Examiner, a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned attorney.

Respectfully submitted,



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Claims Appendix (Independent Claim 1)

1. (Previously presented) A data processor comprising:

one or more functional units arranged to provide an internal processor pipeline,

one or more register files,

a data memory facility having a multibit access port facility,

a snapshot buffer, differing from the one or more register files, which during handling of an interrupt condition accommodates saving, by copying from the one or more register files to respective snapshot buffer elements, state information of various processor state elements, including state information from the internal processor pipeline, and

a controller means arranged to save, upon occurrence of a subsequent interrupt condition during handling of an actual interrupt condition, the state information of various processor state elements currently within the respective snapshot buffer elements in the data memory facility having the multibit access port facility.